CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

Please amend the paragraph beginning on page 7, line 26, and ending on page 7, line 32, line 11, as follows:

Connected in this manner, the circuit acts as a ring oscillator and a chain of logic high and logic lows propagate round. The rate at which the logic high and logic lows propagate depends upon the propagation delay through each latch 10a and 10b. If the delay through latch 10a is T_1 and the delay through latch 10b is T_2 then the oscillation frequency = $1/[2(T_1+T_2)]$.

Please amend the paragraph beginning on page 7, line 33, and ending on page 8, line 11, as follows:

If the delays T_1 and T_2 are made to vary cyclically, with frequency f_{in} , about a value of $1/[2f_{in}] < T_1$ and $T_2 < 1/[2f_{in}]$) such that T_1 increases when T_2 decreases and vice versa, then the logic highs and lows can only propagate round the circuit with a delay of $2/f_{in}$. Any signal that tries to propagate round the circuit any faster or slower than this will automatically be slowed down or speeded up, as the case may be, due to the alternating delay values. In this way, the circuit becomes an oscillator locked at frequency $f_{in}/2$, and thereby forms a frequency divider, since f_{in} is the frequency of the input signal IN/INB. When viewed in this way, the operation of the circuit can be likened to a so-called parametric amplifier.

Please amend the paragraph beginning on page 9, line 32, and ending on page 10, line12, as follows:

Figure 5 schematically shows the input/output characteristic of each amplifier 40a and 40b shown in Figure 4 including hysteresis. The overall negative feedback (due to the coupling from the Q output of the second stage to the DB input of the first) overcomes the positive feedback necessary to create hysteresis of each latch. The effect of this is such that by changing the hysteresis the effective propagation delays (T_1 and T_2) through the amplifiers change, while the strength of the connections between the amplifiers remains constant. In particular, if delays

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T_1 and T_2 are made to vary cyclically, with frequency f_{in} about a value of $1/[2f_{in}]$, (i.e. $1/[2f_{in}] < T_1$ and $T_2 > 1/[2f_{in}]$) such that when T_1 increases T_2 decreases and vice versa then, as in the first embodiment, the logic high and lows can only propagate around a circuit with frequency $f_{in}/2$.